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09/578,895	05/26/2000	Shunpei Yamazaki	0756-2160	8423
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EXAMINER				
GEBREMARIAM, SAMUEL A				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary**Application No.**

09/578,895

Applicant(s)

YAMAZAKI ET AL.

Examiner

SAMUEL A. GEBREMARIAM

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 November 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10, 17-23, 25-27, 29-36, 38, 39, 41, 42, 44-47, 49, 50, 52, 53 and 55-64 is/are pending in the application.
- 4a) Of the above claim(s) 17-23 and 25-27 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 29-31, 33-36, 38, 39, 41, 42, 44-47, 49, 50 and 52-64 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Dispersed or Potential Drawing Review (PTO-842)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 11/23/09; 12/17/09; 7/30/10
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/23/2009 has been entered. An action on the RCE follows.
2. The amendment filed on 11/23/2009 has been entered.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 1010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 5, 33 and 44 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 7,466,293 (293).

Regarding claim 1, (293) claims (claim 3) an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising at least two thin film transistors (293, teaches a switching TFT and current-control TFT); and an electroluminescence element comprising an organic layer (common material for EL device) interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor, and wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two

channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (TFTs inherently have source and drain region, hence impurity regions) and wherein at least the two thin film transistors and the electroluminescence elements are connected in series.

Regarding claim 5, (293) teaches the entire claimed structure of claim 1 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (refer to claim 3).

Regarding claim 33, (293) teaches (claim 3) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising an active layer and at least first and second gate electrodes (two TFTs inherently have two gate electrodes) adjacent to the active layer with a gate insulating film interposed therebetween; a current control element comprising at least two thin film transistors; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the current control element and wherein at least the two thin film transistors and the electroluminescence elements are connected in series (refer to claim 3).

Regarding claim 44, (603) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising at least two thin film transistors; a current control element comprising at least two thin film transistors; and an

electroluminescence element electrically connected to the current control element and the electroluminescence elements are connected in series (refer to claim 3).

5. Claims 1, 5, 8, 33, 35, 41, 44, 46 and 52 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 6,879,309 (309).

Regarding claim 1, (309) teaches (claim 1) an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising at least two thin film transistors; (309, teaches a switching TFT and current-control TFT); and an electroluminescence element comprising an organic layer (common material) interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor, and, wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (LDD regions) and the electroluminescence elements are connected in series (refer to claim 1).

Regarding claim 5, (309) teaches the entire claimed structure of claim 1 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (refer to claim 1).

Regarding claim 8, (309) teaches the entire claimed structure of claim 1 above including wherein each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a drain region or the impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap the gate electrodes of the first thin film transistor and wherein the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly (refer to claim 1).

Regarding claim 29, (309) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising at least two thin film transistors; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor, wherein the first thin film transistor comprises an active layer in which at least two channel regions connected in series are formed with an impurity region interposed therebetween, and wherein each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and wherein the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly and the electroluminescence elements are connected in series (refer to claim 1).

Regarding claim 30, (309) teaches substantially the entire claimed structure of claims 2 and 3 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (claim 1).

Regarding claims 33 and 35, (309) claims (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising at least two thin film transistors adjacent to the active layer with a gate insulating film interposed therebetween; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected the current control element (refer to claim 1).

Regarding claim 41, (309) teaches (claim 1) an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising an active layer and at least first and second gate electrodes adjacent to a the active layer with a gate insulating film interposed therebetween; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the current control element, wherein each of the switching element and the current control element has at least one lightly doped impurity region where, wherein the lightly doped impurity region of the

switching element does not overlap a gate electrode of the switching element and wherein the lightly doped impurity region of the current control element overlaps a gate electrode of the current control element at least partly.

Regarding claims 44, 46 and 52, (309) teaches (claim 1) the entire claimed structure of claim 41 above including an electroluminescence display device comprising: a substrate; and a plurality of pixels over the substrate, each of the plurality of pixels comprising: a switching element comprising at least two thin film transistors; a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the current control element.

6. Claims 1-10, 29-31, 33-36, 38-39, 41-42, 44-47, 49-50, 52-53 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 17-30 of US patent No. 7,642,559 (559).

Regarding claims 1-10, 29-30, 33-35, 38, 41-42, 44-46, 49 and 52 (559) teaches (claims 1-10) an electroluminescence display device comprising: a substrate (the EL device is inherently formed on a substrate); a plurality of pixels over the substrate, each of the plurality of pixels comprising: a first thin film transistor; a second thin film transistor comprising at least two thin film transistors; and an electroluminescence element comprising an organic layer interposed between a pair of electrodes, wherein one of the pair of electrodes is electrically connected to the second thin film transistor,

and wherein the first thin film transistor comprises at least two channel regions in an active layer (switching transistor has two TFTs and hence two channel regions), at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions (LDD regions) wherein at least the two thin film transistors and the electroluminescence element are connected in series. Furthermore (933) teaches that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of $W2/L2 > 5 \times W1/L1$ establishes where a channel length of the second thin film transistor is $L2$ (0.1-50 μ m), a channel width of the second thin film transistor is $W2$ (0.5 to 30 μ m), a channel length of the first thin film transistor is $L1$ (0.2 to 18 μ m) and a sum of each of lengths of the channel regions of the width of the first thin film transistor is $W1$ (0.1 to 5 μ m) (claim 3). In addition (933) teaches (claims 5-10) a current control element comprising a gate electrode electrically connected to the switching element; and an electroluminescence element electrically connected to the current control element, wherein each of the switching element and the current control element has at least one lightly doped impurity region where, wherein the lightly doped impurity region of the switching element does not overlap a gate electrode of the switching element and the lightly doped impurity region of the current control element overlaps a gate electrode of the current control element at least partly. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of pixels in the structure of (933), in order to form a functional display device. Furthermore (933)

teaches substantially the entire claimed structure of claims 29, 33, 41, 44, 49 and 52 above including the substrate comprises a material selected from the group consisting of a glass, a glass ceramic, a quartz, a silicon, a ceramic, a metal, and a plastic (refer to claim 22 and 29).

7. Claims 2-4, 34, 38-39, 45, 49 and 50 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 10/980,603 (603) in view of Luo, US patent No., 4,040,073.

Regarding claims 2, 3-4, 9-10, 34, 38, 45 and 49 (603) teaches substantially the entire claimed structure of claim 1 except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of $W2/L2 > 5 \times W1/L1$ establishes where a channel length of the second thin film transistor is $L2$ (0.1-50 μ m), a channel width of the second thin film transistor is $W2$ (0.5 to 30 μ m), a channel length of the first thin film transistor is $L1$ (0.2 to 18 μ m) and a channel width of the first thin film transistor is $W1$ (0.1 to 5 μ m).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a channel width of the first thin film transistor as claimed as taught by Luo in the structure of (603) in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of (603) in order to form a device with improved stability (col. 2, lines 16-25).

Regarding claims 6 and 7, (603) teaches substantially the entire claimed structure of claims 2 and 3 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (claim 1).

Regarding claims 39 and 50, (603) teaches substantially the entire claimed structure of claims 2-3, 38 and 49 above including the substrate is glass (12, fig. 1, Luo).

8. Claims 2-4, 31, 34, 36, 38-39, 42, 45, 47, 49, 50 and 53 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-18 of US 6,879,309 (309) in view of Luo, US patent No., 4,040,073.

Regarding claims 2, 3-4, 9-10, 34, 38, 45 and 49 (391) teaches substantially the entire claimed structure of claims 1 except explicitly stating that a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor or wherein an equation of $W2/L2 > 5 \times W1/L1$ establishes where a channel length of the

second thin film transistor is L2 (0.1-50 μ m), a channel width of the second thin film transistor is W2 (0.5 to 30 μ m), a channel length of the first thin film transistor is L1 (0.2 to 18 μ m) and a channel width of the first thin film transistor is W1 (0.1 to 5 μ m).

Luo teaches a switching thin film transistor T1 and a current control TFT T2, where the channel width can be adjusted depending on the function of the device (col. 3, lines 45-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust a channel width of the second thin film transistor and a channel width of the first thin film transistor as claimed as taught by Luo in the structure of (309) in order to form a device with improved stability (col. 2, lines 16-25).

Furthermore parameters such as channel length and channel width in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the channel length and channel width as claimed in the structure of (309) in order to form a device with improved stability (col. 2, lines 16-25).

Regarding claims 6 and 7, (309) teaches substantially the entire claimed structure of claims 2 and 3 above including the first thin film transistor is a switching thin film transistor and the second thin film transistor is a current control thin film transistor (claim 1).

Regarding claims 9 and 10, (309) teaches substantially the entire claimed structure of claims 2 and 3 above including wherein each of the first and second thin film transistors has at least one lightly doped impurity region between a channel region and one of a drain region or the impurity regions wherein the lightly doped impurity region of the first thin film transistor does not overlap a gate electrode of the first thin film transistor and the lightly doped impurity region of the second thin film transistor overlaps a gate electrode of the second thin film transistor at least partly (refer to claim 1).

Regarding claims 31, 36, 42, 47, 50 and 53, (309) teaches substantially the entire claimed structure of claims 29, 33, 41, 44, 49 and 52 above except explicitly stating that the wherein the substrate comprises a material selected from the group consisting of a glass, a glass ceramic, a quartz, a silicon, a ceramic, a metal, and a plastic.

Luo teaches an electroluminescence device that is based on a glass substrate (12) in order to form a device with improved stability.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electroluminescence device of (309) on a glass substrate as taught by Luo in order to form a device with improved stability.

Response to Arguments

9. Applicant's arguments with respect to claims 1-10, 29-31, 33-36, 38-39, 41-42, 44-47, 49-50, 52-53 and 55-64 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAMUEL A. GEBREMARIAM whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-167070. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Samuel A Gebremariam/

Examiner, Art Unit 2811

/SAG/

October 24, 2010